DCIS 2026 • ERICEIRA, PORTUGAL

TECHNICAL PROGRAM



18–20 NOVEMBER 2026

XLI Conference on Design of Circuits and Integrated Systems

68 oral papers • 16 posters • 16 PhD Forum contributions

DCIS 2026 / CONFERENCE INFORMATION

ABOUT THE CONFERENCE

41st Conference on Design of Circuits and Integrated Systems • Ericeira, Portugal

THE CONFERENCE

DCIS is an international forum for researchers and industry professionals working on micro- and nano-electronic circuits and integrated systems. The conference promotes the exchange of ideas, application experiences and recent advances in the modelling, design, implementation and testing of devices, circuits and systems.

DCIS 2026 AT A GLANCE

WHEN
18–20 November 2026

WHERE
Hotel Vila Galé Ericeira, Ericeira, Portugal

TECHNICAL PROGRAM
68 oral papers across 18 sessions / 3 tracks; 16 posters; 16 PhD Forum contributions

COMPLEMENTARY ACTIVITIES
3 keynote talks, sponsor presentations, panel discussion and social events

SCOPE

Analog and mixed-signal design · RF circuits · EDA tools · hardware security · power and energy management · reconfigurable computing · AI-enabled circuits · emerging devices and technologies.

ORGANIZING COMMITTEE

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DCIS 2026 / MESSAGE FROM THE GENERAL CO-CHAIRS

WELCOME TO DCIS 2026

18–20 November 2026 • Ericeira, Portugal

On behalf of the Organizing Committee, it is our pleasure to welcome you to the 41st Conference on Design of Circuits and Integrated Systems (DCIS 2026), taking place in the coastal town of Ericeira, Portugal.

DCIS brings together researchers, engineers, industry representatives and students to present new ideas, discuss emerging technologies and strengthen collaborations across the fields of micro- and nano-electronics. This year's program reflects the breadth of our community, from analog and RF circuits to embedded systems, design automation, hardware security, energy management and novel computing paradigms.

The technical program features 68 oral papers organized into 18 sessions across three parallel tracks, alongside 16 poster presentations and 16 PhD Forum contributions. Three keynote lectures, special sessions, sponsor presentations and a panel discussion complement the scientific exchange. We particularly welcome the contribution of early-career researchers and look forward to the discussions that their work will generate.

Ericeira provides an inspiring setting for the conference. Beyond the technical sessions, we hope participants will enjoy the opportunities to meet colleagues, exchange perspectives and discover the cultural and natural surroundings of the Portuguese coast.

We warmly thank the authors, session chairs, keynote speakers, reviewers, committee members, sponsors and volunteers whose contributions make DCIS 2026 possible. We wish you an engaging and productive conference, rich in ideas and new professional connections.

Fábio Passos and Marcelino Santos

DCIS 2026 General Co-Chairs

PROGRAM OVERVIEW

Conference schedule • Ericeira, Portugal • 18–20 November 2026

WEDNESDAY, NOVEMBER 18, 2026

08:00–08:30	Registration
08:30–09:00	Opening Session
09:00–10:00	Keynote 1: Alberto Rodriguez-Perez
10:00–10:30	Coffee Break
10:30–12:00	Sessions 1–3 | Parallel tracks
12:00–13:30	Lunch
13:30–15:00	Sessions 4–6 | Parallel tracks
15:00–15:30	Coffee Break / PhD Forum / Posters
15:30–17:00	Sessions 7–9 | Parallel tracks
19:30	Welcome Reception (Dinner)

THURSDAY, NOVEMBER 19, 2026

09:00–10:00	Keynote 2: Francesc Moll
10:00–10:30	Coffee Break / PhD Forum / Posters
10:30–12:00	Sessions 10–12 | Parallel tracks
12:00–13:30	Lunch
13:30–15:00	Sessions 13–15 | Parallel tracks
15:00–15:30	Coffee Break / PhD Forum / Posters
15:30–16:10	Sponsors Presentations
16:10–17:30	Panel: Will AI kill us? The impact of AI in circuit/system design
18:00	Social Event + Gala Dinner (start)

FRIDAY, NOVEMBER 20, 2026

09:00–10:00	Keynote 3: Bram Nauta
10:00–10:30	Coffee Break / PhD Forum / Posters
10:30–12:00	Sessions 16–18 | Parallel tracks
12:00–13:30	Lunch
13:30–15:00	Competence Centers Presentation + Closing Session

Plenary speakers: page 6. Oral sessions: pages 7–12. Posters and PhD Forum contributions: pages 13–14.

PLENARY SPEAKERS

Plenary sessions • 09:00–10:00 • Hotel Vila Galé Ericeira

PLENARY 1 / WEDNESDAY, 18 NOVEMBER / 09:00–10:00

Alberto Rodriguez-Perez · KD (kd.tech)

"Bringing Optical Communications to Automotive: Transistor-Level Design is Just the Starting Point"

Transitioning a high-speed microelectronics concept from a startup vision to a high-volume, automotive-grade reality demands far more than sound circuit topology: it requires complete ownership of technology, silicon IP, and the backend supply chain.

This keynote traces the evolution of KD (kd.tech) as it pioneered rugged optical communication links for harsh vehicle environments. Attendees will follow the company's trajectory from a fabless startup to an integrated automotive Tier-2 supplier. To satisfy the stringent reliability, functional safety, and cost requirements of the automotive sector, KD transitioned to designing proprietary high-speed transceiver IPs, developing custom optoelectronic packaging, and deploying an in-house assembly and production test line.

The talk unpacks the practical realities of high-speed AMS design under automotive environmental extremes, the often-underestimated challenges of optical packaging and co-design, and how the traditional IC designer's role expands when a company takes direct command of manufacturing and quality control.

PLENARY 2 / THURSDAY, 19 NOVEMBER / 09:00–10:00

Francesc Moll · UPC / BSC

"Beyond the Logic Core: RISC-V, Mixed-Signal Bottlenecks, and the Path to Sovereign European HPC"

High-Performance Computing (HPC) sits at the epicenter of technological sovereignty, driving everything from exascale AI and climate modeling to national security. While initiatives like the European Processor Initiative (EPI), EUPilot, DARE, and the Barcelona Zettascale Lab have successfully demonstrated that open-standard RISC-V logic (CPUs, VPUs, and AI accelerators) can power future supercomputers, a critical reality remains: compute silicon does not exist in a vacuum.

A sovereign CPU or vector unit is only as capable as the system supporting it. This keynote explores the architectural anatomy of sovereign HPC compute engines and confronts the "missing pieces" in the European design ecosystem. We examine why the key bottlenecks to true hardware independence are shifting from digital logic to advanced analog/mixed-signal IP (PHYs for HBM3/4, LPDDRx, PCIe, and UCIe die-to-die chiplet interfaces), open EDA scaling, and 2.5D/3D packaging realities. Finally, we highlight the central role of Academia and Research Technology Organizations (RTOs) in training the next generation of microelectronic engineers, bridging the lab-to-fab gap through pilot lines, and using open-source IP to transform theoretical research into physical, production-ready silicon.

PLENARY 3 / FRIDAY, 20 NOVEMBER / 09:00–10:00

Bram Nauta · University of Twente

"High Risk, No Gain"

Conventional radio receivers place amplifiers at the front of the signal chain, a component still considered indispensable. This talk argues that amplifiers may be unnecessary in many cases and that removing them unlocks meaningful performance and efficiency gains.

The first part introduces mixer-first receiver architectures, which replace the low noise amplifier at the antenna with a low-loss passive mixer. Combined with N-path filtering, a powerful technique from a forgotten era, these architectures deliver selectivity directly at the antenna input, providing strong interference resilience without active amplification.

The second part extends this philosophy to the baseband domain. A fundamental thermodynamic argument shows that a comparator and an amplifier require the same energy when normalized for noise and bandwidth. Conventionally, an amplifier chain amplifies the signal to the 1V range, to drive an ADC. This theory shows that the ADC can in principle process small signals directly. It will dissipate more power to maintain noise performance while reclaiming the power previously spent in the amplifier chain driving the ADC.

Together, these ideas outline a roadmap toward fully passive receiver frontends and may ultimately challenge conventional receiver architectures.

WEDNESDAY • 18 NOVEMBER

10:30–12:00 | PARALLEL TECHNICAL SESSIONS

SESSION 01 / TRACK 1 Chair: Koldo Basterretxea

SS1 — Neuromorphic Circuits, Systems, and Technologies (Special Session)

#1315 **Memristor-based Liquid Spiking Neural Network**
Jorge Iglesias, Antonio Calomarde and Antonio Rubio

#3066 **Dual Evaluation of SNN-Based AoA Estimators Across Commercial and Custom Neuromorphic Hardware**
Alvaro Poveda Ruiz, Cristina Bermúdez-Martín and Pablo Ituero

#3610 **A Conductance-Based Design Methodology for Single-Transistor Organic Electrochemical Neurons**
Carlos Francisco Alvarez-Meythaler, Carme Martínez-Domingo, Cecilia Jiménez-Jorquera and Josep Maria Margarit-Taulé

#1542 **A Neuromorphic 65 nm Analog Front-End with Verilog-A Memristive Spike-Timing-Dependent Plasticity Learning**
Diogo Caetano, André Santos, Mário Silva, Alexandre Santos, Vasco Nunes, Marcelino Santos and Sharon Bikobo

SESSION 02 / TRACK 2 Chair: Marcelino Santos

Voltage/Current References & Low-Power Analog

#9155 **A Resistor-less Reference Circuit Generating Temperature-Compensated Current and Voltage Outputs down to 0.7-V Supply Voltage**
Francesco Gagliardi and Michele Dei

#9201 **A Resistorless Subthreshold Voltage Reference Using a PMOS Translinear Loop**
Claudiu Nechifor, Américo Dias, Laurentiu Matei, Paulo Martins and Daniel Oliveira

#2889 **A 1-V 5-uW OTA Based on Shunt LCMFB with 5.2-V/us SR and 2.1-MHz GBW for a 70-pF Load**
Antonio Lopez-Martin and Jose M. Algueta Miguel

#4887 **A CMOS Platform for High-Current Driving and On-Chip Characterization of NIR micro-LEDs for Microbot Applications**
Rafael Ferreira, Accel Abarca, Carlos Lisboa, Juan Moya, Helder Avelar, Nuamam Kutty, Juan Silva, Bruno Romeira and João Piteira

SESSION 03 / TRACK 3 Chair: Josep Maria Lopez Villegas

RF & mm-Wave Circuits

#1988 **SRF-Aware Surrogate-Assisted Modeling and Optimization of Integrated 8-Shaped RF Inductors**
Duarte Marques, João Gonçalves, Ricardo Martins and Fábio Passos

#8822 **Physics-Aware Surrogate Modeling for RF Integrated Inductors**
José Manuel Cruz Acosta, Marta Tejera López, David Galante-Sempere, Javier del Pino and Sunil L. Khemchandani

#9061 **A 22FDX CMOS Feedback-Cascode UWB LNA for IEEE 802.15.4z Automotive Applications**
Miguel Quevedo Pérez, David Galante Sempere, Jose Luis Saiz Pérez, Francisco Javier del Pino Suárez and Sunil Khemchandani Lalchand

#6889 **Low-Power CMOS PLL employing a Capacitance Multiplier Technique and a Current-Compensated Charge Pump**
Pedro Duarte, João Oliveira, Hugo Serra and Luís Oliveira

WEDNESDAY • 18 NOVEMBER

13:30–15:00 | PARALLEL TECHNICAL SESSIONS

SESSION 04 / TRACK 1 Chair: Javier Uceda

Power Management, Communication & Automotive Analog

#8655 **A Class-E Power Amplifier and Rectifier for Wireless Power Transfer Applications**
Gonçalo Antunes, Gonçalo Rodrigues and Fábio Passos

#3826 **An Automated and Cost-Effective Battery Characterization Framework Using Standard Laboratory Instrumentation**
Mariana A. Pinto, Henrique A. Pocinho, Miguel D'Avó Luís, Tiago H. Moita, Marcelino B. dos Santos and Fábio Passos

#4296 **A Robust Isolated Communication Architecture for Automotive BMS under BCI-Induced Noise**
Jonghun Kim, Seung-Yeon Kim, Seung-Wuk Baek, Seong-Ho Oh, Si-Kwang Lee and Sung-Hoon Bang

SESSION 05 / TRACK 2 Chair: Antonio Lopez

Sensor Interfaces & Instrumentation I

#3355 **A ±0.375 ◦C, 40 µs BJT-Based Temperature Sensor with Charge-Domain Integrator-Assisted SAR ADC**
Francisco Apolinário, Diogo Gonçalves, André Romão, Marcelino Santos and Fábio Passos

#4760 **Staggered BPF for Simultaneous Multi-Sine Impedance Spectroscopy**
Juan María Nogales, Israel Corbacho, Francisco Romero, Miguel Á. Domínguez and Juan Manuel Carrillo

#5452 **Generalized Magnitude-Ratio and Phase-Difference Detection Method for Low-SoC Li-Ion Battery EIS**
Juan María Nogales, Israel Corbacho, Francisco Romero, Miguel Á. Domínguez and Juan Manuel Carrillo

#9263 **Design Space Exploration of CMOS Transimpedance Amplifiers for Ultra-Low Current THz Imaging Sensors**
Fernando Martos García, Javier de Mena Pacheco, María Luisa López Vallejo and Jesús Grajal de la Fuente

SESSION 06 / TRACK 3 Chair: Miquel Roca

Sensor Interfaces & Instrumentation II

#4656 **A monolithic SPAD lifetime-imaging SoC with RISC-V-based programmable on-sensor lifetime extraction**
Guillem Prenafeta, Sergio Moreno, Jan Castillo and Angel Dieguez

#9998 **Towards an Integrated Photonics-based Wavefront Sensor (IP-WFS) for Solar Adaptive Optics: A Numerical Simulation Framework**
Diego Portero Rodríguez, Hugo García-Vázquez, José Javier Díaz García, Luis Fernando Rodríguez Ramos, José Alfonso López Aguerri and Marcos Reyes García-Talavera

#5006 **Jitter Optimization of Large-Area SiPM Analog Readout Via Simultaneous Power and Noise Matching**
Juan José Silva García, Jose Maria López Villegas, David Gascón Fora, Jose Maria Fernandez-Tenllado Arribas and Sara Portero Castillo

WEDNESDAY • 18 NOVEMBER

15:30–17:00 | PARALLEL TECHNICAL SESSIONS

SESSION 07 / TRACK 1 Chair: Celia Lopez

Emerging Devices: Memristors & Neuromorphic Circuits

#1006 **A Framework for RRAM Characterization and Model Calibration**
Vahab Mahboubi, Daniel Arumi Delgado, Álvaro Gómez Pau, Rosa Rodríguez Montañés, Victor Suñe, Eduardo Pérez, Keerthi Dorai Swamy Reddy, Christian Wenger and Salvador Manich Bou

#8922 **Drift–Diffusion Kinetics-Based Memristive Feature Extraction for End-to-End Hardware-Aware Inference**
Masoumeh Mohammadidoghozloo, Jose Diogo Costa Teixeira, Víctor Leborán, Fernando Rafael Pardo Seco, Francisco Rivadulla, Victor Brea and Paula López

#5996 **A Voltage-to-Time Readout Architecture for Fully Analog Memristive SNNs**
Èlia Mateu Barriendos, Álvaro Gómez-Pau, Josep Rius, Daniel Arumí, Rosa Rodríguez-Montañés and Salvador Manich

SESSION 08 / TRACK 2 Chair: Eugenio Villar

Edge AI Hardware & Neural Architectures

#7542 **A Compact FVF-Based Analog Neuron in 28nm CMOS for Edge AI**
Elena Benítez López, Clara Isabel Luján Martínez, Enrique López Morillo, Ramón González Carvajal, Juan Antonio Gómez Galán and Fernando Muñoz Chavero

#5883 **Fully Gradient-Free CoDeepNEAT for Hardware-Oriented Neural Architecture Search**
Enrique Maseda and Andrés Otero

#7987 **A Balanced Accuracy–Size Metric for MLP Optimization**
Lluc Crespí-Castañer, Joan Font-Rosselló, Alejandro Morán, Christiam Camilo Franco Frasser, Miquel Roca and José Luis Rosselló

#4184 **FPGA Implementation of an Oscillator-Based Ising Machine for Solving Large MAX-CUT Problems**
Stefano Crescenza, Johnny Öberg and Ana Rusu

SESSION 09 / TRACK 3 Chair: Nuno Neves

FPGA-Based Signal Processing

#0796 **A Cross-Domain Scalable FFT Implementation for Heterogeneous AMD Versal ACAP Systems**
Francisco González-Castro, Fernando Flores García, Maria Dolores Valdés Peña and José Manuel Villapún Sánchez

#2949 **A Scalable Multichannel FFT Implementation for Real-Time Biological Signal Processing**
Manuel Morato, Nicolás Medrano and Belén Calvo

#0437 **Parallelizing Convolutional Neural Network Inference on the Propeller 2 Low-Power Multicore Microcontroller**
Alejandro del Rio, Nicolás Medrano Marqués, Belén Calvo López and Manuel Morato

#0068 **A Comparative Evaluation of All-Digital Phase-Locked Loops (ADPLLs) from Literature: FPGA-Based Implementation and Performance Analysis**
Jesús Lázaro, Jaime Jimenez Verde and Armando Astarloa Cuellar

THURSDAY • 19 NOVEMBER

10:30–12:00 | PARALLEL TECHNICAL SESSIONS

SESSION 10 / TRACK 1 Chairs: Miguel Chavarrías and Gustavo M. Callico

SS2 — Case Studies of AI-Enabled Design Methodologies and Application Development in Real-World Scenarios (Special Session)

#7711 **A distributed IR LED system for automatic multi-camera integration within an optical tracking system**
Daniel Yeara Peláez, Manuel Villa, Jaime Sancho, Yingying Gao, Guillermo Vazquez Valle, Pedro Luis Cebrián Castel and Miguel Chavarrías

#7929 **Enabling Run-Time Reconfiguration on FPGAs via Custom ISA Extensions in RISC-V Processors**
Alberto Gago and Alfonso Rodríguez

#4290 **A RISC-V-based SoC Prototype for the Efficient Processing of Generalized ANNs**
Hodei Ganboa, Unai Sainz-Estebanez and Koldo Basterretxea

#5207 **Mind the Offload: Application-Visible Speedup of Biomedical Deep-Learning Workloads on CGRAs**
Daniel Vazquez Iglesias, Isabel Isla, Alejandro Ramirez, Andres Otero and Jose Miranda

SESSION 11 / TRACK 2 Chair: João Casaleiro

Healthcare & Energy-Aware Sensing

#2527 **Lightweight Patient Pose Estimation for Surgical Milestone Detection in Clinical Environments: A YOLO-Pose and MLP-Based Approach**
Jesús Pérez-Llano, Malika Kace, Constantino Barcia, Fernando Setien and Pablo Sanchez

#6744 **Towards an Ultrasound Energy-Harvesting Implantable System with Integrated Power Management and Thermoelectric Actuation**
Nehuel Bernardi Alfama, Aitor Molina Carrion, Neri Ruiz Lupon, Luis Gerardo Parés Manzano, Manel Puig-Vidal, Jordi Colomer-Farrarons and Pere Miribel-Català

#3013 **Ultra-Low-Power Solid-State Energy Harvesting System for Power-over-Fiber**
João Casaleiro and Carlos Carvalho

#3653 **Advancing on Flexible Sensor Design, Instrumentation and Machine Learning Assisted Readout for Soft Applications**
Nelson Castro, Inês Silva, Nikola Perinka, Carlos Costa, Estela Bicho and Senentxu Lanceros-Méndez

SESSION 12 / TRACK 3 Chair: To be confirmed

IoT, Industry 4.0 & Wireless Transceivers

#5719 **An Open-Source Low-Cost Integrated Firmware–Gateway Stack for Scalable and Edge-AI-Ready Industrial IoT**
Luciano Radrigan, Miguel Duran, Sebastian E Godoy, Pedro Toledo and Anibal S Morales

#6165 **A Low-Cost, Low-Power IoT Node for Distributed Railway Track Monitoring with Edge Feature Extraction**
Joaquín Álvarez Molins, Gloria Santiago Viejo, Daniel Narbona Miguel, Jorge Jiménez-Sánchez, Juan Luis Cámara Garrido and Fernando Muñoz Chavero

#6669 **Design and FPGA Implementation of an Adaptive LL-LMS Algorithm for I/Q Imbalance Correction in a Digital Transceiver**
Joao Antunes, João Oliveira and Luís Oliveira

#7720 **TinyML-Based Virtual Sensing for Railway Structural Health Monitoring**
Manuel Fernández-Giráldez, Juan Luque-Girón, Pedro Blanco Carmona, Eduardo Hidalgo-Fort, Juan Luis Cámara-Garrido and Fernando Muñoz-Chavero

THURSDAY • 19 NOVEMBER

13:30–15:00 | PARALLEL TECHNICAL SESSIONS

SESSION 13 / TRACK 1 Chair: Marisa Lopez-Vallejo

RISC-V Systems & Reliability

#7107 **Radiation Tolerance on RISC-V: a technology independent practical case**
Juan-Manuel Galan-Serrano, Aitor Olaizola Panigua, Andoni Irizar Picon and Ainhoa Cortes Vidal

#9267 **A Real-Time Framework for FPGA IP Core Validation of H.264 for Onboard Satellite Systems**
Juan Manuel Vega Mujica, Jorge Sánchez Medina and Roberto Sarmiento Rodríguez

#5430 **Modelling the OP-TEE Invocation Overhead on Arm TrustZone**
Nuno Abreu, Tiago Rocha, Nuno Roma, Nuno Neves and Pedro Tomas

#4547 **Towards Mixed-Criticality RISC-V Systems with VirtIO-Based Inter-Domain Ethernet Communication**
Jonathan López Valdivieso and Andrés Otero

SESSION 14 / TRACK 2 Chair: Ricardo Martins

EDA Tools & AI-Assisted Design

#5091 **Efficient and Reliable On-Premise Language Models-based SVA Generation using Typed Guarded Transition Systems**
Javier Romero, Soledad Escolar, Jesús Barba, Fernando Rincón, Melisa Kuzman and Julián Caba

#8992 **Comparative Analysis of Local LLMs for RTL Code Generation and Modification**
Jesús Lázaro, Ander Núñez, Jaime Jiménez and Armando Astarloa

#3929 **Towards Automatic Analog Integrated Circuit Routing using Fully Convolutional Networks**
Inês Monteiro, Filipe Azevedo, Sandro Rovere, Luca Bortolussi and Ricardo Martins

#6923 **Hardware-Efficient FPGA Deployment of Interpretable Neural Network Controllers for Switched-Mode Power Converters**
Zhi Li, Benjamin Schwabe, Lorenzo Servadei and Robert Wille

SESSION 15 / TRACK 3 Chair: Luis Parrilla

Test, Characterization & Hardware Security

#3425 **Fabrication and Experimental Validation of a DDRFET Device for Hardware Security**
Antonio Manuel Hervás Ramírez, Ruben Ortega Lopez, Luca Donetti, Carlos Márquez Gonzalez and Carlos Navarro Moral

#6207 **AES Decryption Optimization for 32-bit RISC-V Cores Extending the Zknd ISE**
Juan M. Delgado-Romero, Carlos Fernández-García and Carlos J. Jiménez-Fernández

#3305 **A Lightweight C++ Library for HUB-FP Simulation and Testbench Generation**
Alejandro Fuster López and Javier Hormigo

#8313 **Microvolt-Step Stimulus Generation System for Low-Cost ADC Characterization**
Matilde M. S. Augusto, Henrique A. Pocinho, Miguel D'Avó Luís, Tiago H. Moita, Marcelino B. Dos Santos and Fábio Passos

FRIDAY • 20 NOVEMBER

10:30–12:00 | PARALLEL TECHNICAL SESSIONS

SESSION 16 / TRACK 1 Chair: Fábio Passos

ADCs and Analog Circuit Building Blocks

#7334 **A 46.7-mW 10-bit No-Calibration Current-Steering DAC at 5-GS/s in 40-nm CMOS Using a Power-Aware Design Methodology**
Mario Pliego, Juan Manuel Rodríguez-Sánchez, Rocío del Río, Óscar Guerra, Juan Antonio Leñero-Bardallo and Ángel Rodríguez-Vázquez

#8759 **A Wideband Single-Ended-to-Differential Input Buffer With Active-Inductor Loads for Frequency-Interleaved ADCs**
João Santa-Rita, Diogo Novais, João Oliveira and Luís Oliveira

#9598 **A Fully Analog Duty Cycle Corrector for 16 Gb/s UCIe Transmitters in 16 nm FinFET Technology**
David Pinto, Marisa Lopez-Vallejo and Ruzica Jevtic

SESSION 17 / TRACK 2 Chair: Luis Oliveira

Reconfigurable & Radiation-Hardened Systems

#2046 **FPGA acceleration of the Grover's Algorithm with 20 qubits**
Haruto Kurokawa, Minoru Watanabe and Nobuya Watanabe

#8549 **Synchronized operation of a sequential circuit between two optically reconfigurable gate arrays**
Ayumu Ogura, Minoru Watanabe and Nobuya Watanabe

#4224 **Soft-error tolerance of a radiation-hardened JTAG Interface**
Naoki Nagamine, Minoru Watanabe and Nobuya Watanabe

#4842 **Digital Electronic Architecture for SEU-Resilient SpaceWire Communication Node**
Miguel Ángel Salguero Vives, Armando Astarloa Cuellar, Jesús Lazaro Arrotegui, Aitzol Zuloaga Izaguirre and Jaime Jimenez Verde

SESSION 18 / TRACK 3 Chair: Jaime Verde

OTAs, Education & Circuit Design Platforms

#5542 **An Online Learning Platform for Digital Circuits**
Francesc Madrid-Lozano, Xavier Casas Mitjans, Miquel Torner Viñals, Jordi Petit Silvestre and Jordi Cortadella

#5602 **Mondragon: a standard bring-up platform for academic computing ASICs**
Jennifer Hernández, Hugo Safadi, Santi López, Fernando Arreza, Josep Oltra and Francesc Moll

#2857 **A CMOS Translinear Square-Root Circuit with Reduced DIBL-Induced Error in 350 nm and 65 nm Technologies**
Henrique A. Pocinho, Francisco Apolinário, Ricardo Miguel Ferreira Martins, Marcelino B. dos Santos and Jorge Fernandes

#7473 **Fully Complementary OTA with Enhanced Common-Mode Performance**
Julia Aragues, Belen Calvo and Nicolas Medrano

POSTERS & PHD FORUM

32 accepted contributions

POSTER PRESENTATIONS | 16 papers

#1177 **Power optimization of ring oscillator readout circuits for extreme-edge wearable sensors**
Ignacio Beitia, Celia Lopez-Ongil and Susana Paton

#2738 **A Compact Low-Power ADC-Free Readout Circuit for µC-Based Resistive Sensor Microsystems**
João Aguiar and José Machado da Silva

#2759 **A Low-Cost GPIO-Based Method for Large Resistive Sensor Matrix Readout with Minimal Hardware**
Pedro M. Pereira Abreu, Sérgio Abílio Pereira Gonçalves and Estela Bicho

#3089 **Design of a Highly Reliable Power Architecture for Automotive Battery Management System ICs**
Seulkirom Kim, Yoonji Kim, Jonghun Kim, Hyeonyong Jeong, Seungyeon Kim, Sunghoon Bang and Sikwang Lee

#3361 **Hardware-Aware Deployment of Quantized CNNs for Multi-Label Remote Sensing Classification on FPGA**
Antonio J. Suárez Santana, Samuel Torres Fau and Roberto Sarmiento

#3646 **Self-biased startup-less bandgap and voltage regulator circuits for low power applications**
Miguel Ramos, Szymon Gerka and Humberto Fonseca

#4028 **From RGB to Hyperspectral Imaging: Trade-offs in 3D Surface Reconstruction on Embedded Platforms using Structured Illumination**
Adrián Casillas-Sanz, Alberto Martín-Pérez, Jaime Sancho, Manuel Villa, Ana Xinhan Garrido Ruiz, Iván Moreno-Vallejo and César Sanz

#5773 **Architectural Evaluation of Unrolled and Pipenlined Chacha20 in 45 nm Using Open-Source Flow**
Dinis Santos

#6357 **Low-noise OTAs for Micropower Bioamplifiers**
Julia Aragues, Belen Calvo and Nicolas Medrano

#6455 **A Wideband SiGe BiCMOS Modulator Driver Achieving 89 GHz Bandwidth and 2 Vpp Single-Ended Swing for EAM-Based Optical Links**
Catarina Martins, Quang-Binh Pham, Ahmet Cagri Ulusoy and Pedro Rito

#7120 **Analysis of Tunable N-Path Filters for RF Applications**
Marta Tejera López, José Manuel Cruz Acosta, David Galante-Sempere, Javier Del Pino and Sunil Khemchandani

#7723 **Practical Approach to EDSL Based Solutions for Enhancing IP Core Industrialization**
Ander Núñez, Jesús Lázaro, Jaime Jiménez and Armando Astarloa

#7972 **Zkne-Compatible AES Acceleration for 32-bit RISC-V Processors**
Luis Parrilla, Rubén Padial-Allué, Francisco J. Romero, Víctor Toral, Antonio García and Encarnacion Castillo

#8045 **Evaluation of monocular depth estimation models in endoscopic images for tumour brain resection: a phantom study**
Ana Xinhan Garrido Ruiz, Manuel Villa, Adrián Casillas-Sanz, Alejandro Martinez de Ternero, Gonzalo Rosa-Olmeda, Andrea Lozano, Aure Enkaoua and Eduardo Juarez

#8284 **Design of an ADC based on organic transistors for Resource-Constrained Portable Biomedical Systems**
Roger Sole, Laia Antoli, Jordi Sacristán and Eloi Ramon

#8651 **Coverage Enhancement of Battery Cell Open-Wire Diagnosis in BMICs for BMS stack cell Architectures**
Jaewon Choi

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#0192 **Clock Distribution and Calibration in Modern IQ Transceivers for Next-Generation Wireless Systems**
Ruben Marz Martinez

#0922 **Frequency-to-Digital based Readout IC for Next-Generation Medical Imaging Detectors**
Angel Sánchez Navarro

#1455 **Design of Low-Noise and High-Precision CMOS Instrumentation Amplifiers (IAs)**
Victor Marco

#3129 **ONNX-Flow**
José Ferreira

#3267 **Machine Learning-Based Real-Time Ultrasound Pulse-Echo Monitoring of Coating Degradation and Pitting Corrosion**
Marina Perez Diego, Ainhoa Cortés Vidal and Andoni Irizar Picón

#3986 **agnostIP: An Agnostic Mixed-Signal Soft-IP CMOS Design Methodology for Open-Source Repositories**
Jaume Bruguera, Francisco Serra-Graells and Lluís Terés

#5052 **RISC-V System-on-Chip with Unconventional Computing for AI in Edge Computing**
Rui Ferreira, Rui Duarte, Alessandro Savino and Paulo Flores

#5670 **Efficient Digital Architectures to Calculate Convolutional Filters**
Francisco Albertuz

#5897 **On-chip system for simultaneous multi-frequency broadband bioimpedance spectroscopy**
Israel Corbacho Correa

#6081 **Contributions to the development of real-time brain shift compensation algorithms during neurosurgery for enhanced neuronavigation**
Alvaro Falcon, Román Quevedo-Reina and Gustavo M. Callico

#6640 **FPGA-Based Neuromorphic Acceleration for RF Signal Feature Extraction**
Cristina Bermúdez-Martín and Pablo Ituero

#7461 **Low-Power Low-Noise High-Density Digital Readout Integrated Circuits for MWIR PbSe-CMOS High-Speed Imagers**
Eva Maria Deltor, Francisco Serra-Graells and Luis Teres Teres

#8292 **Machine Learning-Assisted Design of RFIC/MMIC Passive Components**
José Manuel Cruz Acosta

#8370 **Design and Behavioural Modelling of a Multi-Standard Digital-to-Analog Converter (DAC) for High-Speed and High-Linearity Applications**
Jose Vicente Casaña Copado

#8489 **Novel methodological frameworks for welfare-aware intelligent aquaculture systems**
Iván Moreno-Vallejo

#9348 **A RISC-V Based Platform for Mixed-Criticality Systems with TSN-Enabled Determinism**
Jonathan López Valdivieso and Andrés Otero